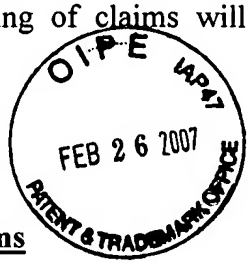
AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.



Listing of Claims

Claims 1-13 (Cancelled)

14. (New) A CPU contained LSI comprising:

a contained CPU;

a first bus connected to the contained CPU;

a second bus connected to an external CPU; and

a bus adjusting circuit disposed between the first bus and the second bus to exclusively control accesses of the external CPU and the contained CPU to a device connected to the first bus;

wherein, when a chip select signal and an address to access the device connected to the first bus from the external CPU are inputted during an access to the device connected to the first bus by the contained CPU, the bus adjusting circuit inputs the address to the first bus from the second bus by releasing a wait signal to permit the external CPU to access the device connected to the first bus and connecting the second bus to the first bus after stopping the access of the contained CPU to the first bus.

15. (New) A CPU contained LSI according to claim 14, wherein when the chip select signal and the address to access the device connected to the first bus from the external CPU are

inputted during an access to the device connected to the first bus by the contained CPU, the bus adjusting circuit transmits a bus release request signal to the contained CPU, and when the bus adjusting circuit receives a bus release completion signal from the contained CPU, the bus adjusting circuit releases the wait signal to permit the external CPU to access the device connected to the first bus.

16. (New) A CPU contained LSI according to claim 15, wherein when a stop of the operation of the contained CPU is set, the bus adjusting circuit permits the external CPU to access the device connected to the first bus without transmitting the bus release request signal to the contained CPU.

17. (New) A CPU contained LSI according to claim 14, wherein a common memory connected to the first bus is provided.

18. (New) A CPU contained LSI according to claim 14, wherein a memory device connected to the first bus is provided for storing a program for operating the CPU contained LSI.

19. (New) A CPU contained LSI according to claim 14, wherein the bus adjusting circuit is provided with an interrupt control circuit for informing of an interruption between the contained CPU and the external CPU.

20. (New) A CPU contained LSI according to claim 19, wherein the interrupt control circuit includes an interrupt factor register having a plurality of bits in which the allocation and setting of bits of an interrupt factor are programmable and a circuit for outputting an interrupt signal.

21. (New) A CPU contained LSI according to claim 18, wherein the memory device connected to the first bus is a RAM and when the CPU contained LSI is started, the external CPU loads the RAM with a program for operating the contained CPU from an external memory connected to the second bus.

22. (New) A CPU contained LSI according to claim 21, wherein the bus adjusting circuit includes a writing address register and a writing data register, and when the external CPU loads the RAM with the program for operating the contained CPU, the external CPU sets the address of the RAM to the writing address register and writes data to be written in the RAM in the writing data register.

23. (New) A CPU contained LSI according to claim 22, wherein the writing address register is incremented every time data is written in the writing data register.